




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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/019,696	06/20/2002	David Finn	70357	3879
23872	7590	07/08/2004		
MCGLEW & TUTTLE, PC 1 SCARBOROUGH STATION PLAZA SCARBOROUGH, NY 10510-0827			EXAMINER VU, QUANG D	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 07/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/019,696	Applicant(s) FINN ET AL.	
	Examiner Quang D Vu	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 March 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 and 15-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7, 15-20, 22 and 24-27 is/are rejected.
- 7) ☒ Claim(s) 21 and 23 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 4,125,810 to Pavio.

Regarding claim 1, Pavio (figures 1-8) teaches a chip carrier for forming a chip module, the chip carrier comprising:

a substrate formed by a carrier film (11); and

connection leads (15) arranged on the substrate (11), the connection leads (conductive strip [15]) extending strip-like in parallel over the substrate (11), the connection leads (conductive strip [15]) comprising electrically conductive connection strands arranged on the substrate (11) in a single plane and extending in a planar direction over an entire longitudinal dimension of the substrate (11) surface and having a longitudinal expansion flush with a surface of the substrate (11) surface.

Regarding claim 2, Pavio teaches the carrier film (11) is provided with at least one additional conductive strand (conductive strip [22]) on a side opposite the connection strands (conductive strip [15]), wherein the insulating carrier film (11) is arranged as an intermediated layer between the connection strands (conductive strip [15]) on the one hand and the conductive

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strand (conductive strip [22]) on the other. Therefore, it inherently teaches the carrier film is provided with at least one additional conductive strand (conductive strip [22]) on a side opposite the connection strands (conductive strip [15]) to generate a capacitance.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 15, 20 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 5,888,429 to Lovell.

Regarding claim 1, Lovell (figures 1-3) teaches a chip carrier for forming a chip module, the chip carrier comprising:

a substrate formed by a carrier film (3); and

connection leads (2) arranged on the substrate (3), the connection leads (conductive strip [2]) extending strip-like in parallel over the substrate (3), the connection leads (conductive strip [2]) comprising electrically conductive connection strands arranged on the substrate (3) in a single plane and extending in a planar direction over an entire longitudinal dimension of the substrate (3) surface and having a longitudinal expansion flush with a surface of the substrate (3) surface.

Regarding claim 15, Lovell teaches the electrically conductive connection strands (conductive strip [2]) are independent and separate elements from the substrate (3).

Regarding claim 20, Lovell (figures 1-3) teaches a chip carrier arrangement formed by the process steps comprising:

providing a carrier film (3) having a longitudinal dimension;

providing a plurality of electrically conductive connection strands (conductive strip [2]), the electrically conductive connection strands (conductive strip [2]) being provided separately and independently from the carrier film (3);

attaching electrically conductive connection strands (conductive strip [2]) onto the carrier film (3) as stripes extending substantially in parallel over the carrier film (3), the electrically conductive connection strands (conductive strip [2]) being arranged on the carrier film (3) in a substantially single plane and extending in a planar direction over the entire longitudinal dimension of the carrier film (3).

Regarding claim 26, Lovell teaches the attaching of the electrically conductive connection strands (conductive strip [2]) onto the carrier film (3) is performed with adhesive (an adhesive [61] as shown in figure 3).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 3-4, 6 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,888,429 to Lovell in view of US Patent No. 5,176,853 to Sarma et al.

Regarding claim 3, Lovell differs from the claimed invention by not showing the connection strands are at least sectional provided with a connecting material coating for contacting with the contact metallizations of a chip. However, Sarma et al. (figure 9) teach the connection strands (509) are at least provided with a connecting material layer (609) for coating with the contact metallizations of a chip (209) on the substrate (409). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sarma et al. into the device taught by Lovell because it holds the chip in place. The combined device shows the connection strands are at least sectional provided with a connecting material coating for contacting with the contact metallizations of a chip.

Regarding claim 4, Lovell differs from the claimed invention by not showing the connection strands are at least sectionally provided with a contact metallization for contacting with the contact metallizations of a chip. However, Sarma et al. (figure 9) teach the connection strands (509) are at least sectional provided with a contact metallizations (309) for contacting with the contact metallizations of a chip (209) on the substrate (409). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sarma et al. into the device taught by Lovell because it holds the chip in place. The combined device shows the connection strands are at least sectionally provided with a contact metallization for contacting with the contact metallizations of a chip.

Regarding claim 6, Lovell (figures 1-3) teaches a chip module, comprising:

a chip carrier comprising a substrate formed by a carrier film (3) and connection leads (conductive strip [2]) arranged on the substrate (3), the connection leads (conductive strip [2]) comprising stripes and extend parallel over the substrate (3), the connection leads (conductive strip [2]) comprising electrically conductive connection strands arranged on the substrate (3) in a single plane and extending in a planar direction over the substrate (3) surface and having a longitudinal expansion flush with the substrate surface, the electrically conductive connection strands (conductive strip [2]) being independent and separate elements from the substrate (3).

Lovell differs from the claimed invention by not showing connecting surfaces with elevated contact metallizations, the contact metallizations being in contact with a top side of the connection strands facing away from the carrier film. However, Sarma et al. (figure 9) teach connecting surfaces with elevated contact metallizations (609), the contact metallizations (609) being in contact with a top side of the connection strands (509) facing away from the carrier film (409). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sarma et al. into the device taught by Lovell because it provides interconnection in the upper surface of the substrate with other device. The combined device shows connecting surfaces with elevated contact metallizations, the contact metallizations being in contact with a top side of the connection strands facing away from the carrier film.

Regarding claim 22, Lovell differs from the claimed invention by not showing providing a chip with contact metallizations and connecting the contact metallizations with the electrically conductive strands. However, Sarma et al. (figure 9) teach a chip (20) with contact metallizations (309) and connecting the contact metallizations (309) with the electrically

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conductive strands (609) on the substrate (409). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Sarma et al. into the device taught by Lovell because the chip can be hold in place.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,888,429 to Lovell in view of US Patent No. 6,326,233 to Hashimoto.

Regarding claim 5, Lovell differs form the claimed invention by not showing the connection strands are connected with the terminals of a coil unit. However, Hashimoto (figures 7-8) teaches the connection strands (20) are connected with the terminals of a coil unit. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Hashimoto into the device taught by Sarma et al. because it increase the productivity of the device. The combined device shows the connection strands are connected with the terminals of a coil unit.

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lovell in view of Sarma et al., and further in view of US Patent No. 6,326,233 to Hashimoto.

Regarding claim 7, the disclosures of Lovell and Sarma et al. are discussed as applied to claim 6 above.

Sarma et al. differ from the claimed invention by not showing the connection strands are connected with the terminals of a coil unit. However, Hashimoto (figures 7-8) teaches the connection strands (20) are connected with the terminals of a coil unit. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to

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incorporate the teaching of Hashimoto into the device taught by Lovell and Sarma et al. because it increase the productivity of the device. The combined device shows the connection strands are connected with the terminals of a coil unit.

9. Claims 16-17, 19, 24-25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,888,429 to Lovell.

Regarding claims 16-17, Lovell differs from the claimed invention by not showing the carrier film and the electrically conductive strands have a flexibility to be provided in rolls in the embodiment of figures 1-3. However, Lovell teaches the carrier film (3) and the electrically conductive strands (conductive strip [2]) have a flexibility to be provided in rolls in the embodiment of figure 5. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include limitation shown in the embodiment of figure 5 into the embodiment of figures 1-3, since it is desirable for them to have functionality.

Regarding claim 19, Lovell differs from the claimed invention by not showing the carrier film and attached the electrically conductive strands have a flexibility to be wound into a roll in the embodiment of figures 1-3. However, Lovell teaches the carrier film (3) and attached the electrically conductive strands (conductive strip [2]) have a flexibility to be wound into a roll in the embodiment of figure 5. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include limitation shown in the embodiment of figure 5 into the embodiment of figures 1-3, since it is desirable for them to have functionality.

Regarding claims 24-25, Lovell differs from the claimed invention by not showing the carrier film and attached the electrically conductive strands have a flexibility to be wound into a

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roll in the embodiment of figures 1-3. However, Lovell teaches the carrier film (3) and attached the electrically conductive strands (conductive strip [2]) have a flexibility to be wound into a roll in the embodiment of figure 5. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include limitation shown in the embodiment of figure 5 into the embodiment of figures 1-3, since it is desirable for them to have functionality.

Regarding claim 27, Lovell teaches the attaching of the electrically conductive connection strands (conductive strip [2]) onto the carrier film (3) is performed with adhesive (an adhesive [61] as shown in figure 3).

Lovell differs from the claimed invention by not showing the carrier film and attached the electrically conductive strands have a flexibility to be wound into a roll in the embodiment of figures 1-3. However, Lovell teaches the carrier film (3) and attached the electrically conductive strands (conductive strip [2]) have a flexibility to be wound into a roll in the embodiment of figure 5. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include limitation shown in the embodiment of figure 5 into the embodiment of figures 1-3, since it is desirable for them to have functionality.

10. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lovell in view of Sarma et al.

Regarding claim 18, the disclosures of Lovell and Sarma et al. are discussed as applied to claim 6 above.

Lovell differs from the claimed invention by not showing the carrier film and the electrically conductive strands have a flexibility to be provided in rolls in the embodiment of

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figures 1-3. However, Lovell teaches the carrier film (3) and the electrically conductive strands (conductive strip [2]) have a flexibility to be provided in rolls in the embodiment of figure 5. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include limitation shown in the embodiment of figure 5 into the embodiment of figures 1-3, since it is desirable for them to have functionality.

Allowable Subject Matter

Claims 21 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

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the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
June 28, 2004


Donghee Kang
Primary Examiner
A-U. 2811